WHAT IS CLAIMED IS:

1. A logic circuit comprising at least one input, one output and a delay fault circuit, said delay fault circuit including:

a first standard scan cell;

a combinational test point positioned immediately after the first standard scan cell in a scan chain; and

a second standard scan cell positioned immediately after the combinational test point in the scan chain.

2. The logic circuit of claim 1, where the combinational test point is positioned to prevent shift dependency between the first standard scan cell and the second standard scan cell.

3. The logic circuit of claim 1, where the first and second standard scan cells are flip-flops.

4. The logic circuit of claim 1, where the combinational test point comprises an AND gate.

5. The logic circuit of claim 1, where the combinational test point comprises an OR gate.

6. The logic circuit of claim 1, where the combinational test point comprises an AND-OR gate.

7. The logic circuit of claim 1, where the logic circuit is testable under a full standard scan environment.

8. The logic circuit of claim 1, where the logic circuit is testable under a partial standard scan environment.

9. The logic circuit of claim 1, where the logic circuit includes at least one enhanced scan cell.

10. The logic circuit of claim 1, where the circuit is structured so that at least one stuck-at fault in the circuit can be tested.

11. The logic circuit of claim 1, where the circuit is structured so that at least one delay fault in the circuit can be tested.

12. A logic circuit comprising at least one input, one output and a delay fault circuit, said delay fault circuit including:

a first standard scan cell;

a test point positioned immediately after the first standard scan cell in a scan chain; and

a second standard cell positioned immediately after the test point in the scan chain,

where the test point is positioned to prevent shift dependency identified to occur between the first and second standard scan cells in the delay fault circuit.

13. The logic circuit of claim 12, where the position of the test point is determined based on a functional analysis of the circuit.

14. The logic circuit of claim 12, wherein the test point is a dummy scan flip-flop in a scan chain that does not provide input to any primary inputs in the logic circuit.

15. The logic circuit of claim 12, wherein the test point is a combinational test point.

16. The logic circuit of claim 12, wherein the position of the test point is determined by:

identifying dependency untestable transition delay faults;

for every such fault,

generating a test cube pair for the fault if the fault has a minimum test generation cost, and

if there is no conflict with any other test cube pair in a current test cube pair set, adding the test cube pair into the current test cube pair set and updating a current test point vector based on the current test cube pair set; and

generating a global test point vector based on the current test point vector, where the global test point vector specifies the position where the test point should be inserted.

17. The logic circuit of claim 16, where the global test vector also specifies what type of test point should be inserted.

18. A method of testing a logic circuit comprising:

loading a first test pattern into a first standard scan cell in a scan chain;

loading an output of the first standard cell into a combinational test point in the scan chain; and

loading an output of the combinational test point into a second standard scan cell in the scan chain.

19. The method of testing a logic circuit as in claim 18, where the combinational test point prevents shift dependency between the first standard scan cell and the second standard scan cell.

20. The method of claim 18, where the logic circuit is testable under a full standard scan environment.

21. The method of claim 18, where the logic circuit is testable under a partial standard scan environment.

22. The method of claim 18, where the logic circuit includes at least one enhanced scan cell.

23. The method of claim 18, where at least one stuck-at fault in the logic circuit is tested.

24. The method of claim 18, where at least one delay fault in the logic circuit is tested.

25. The method of claim 18, where the combinational test point comprises an AND gate.

26. The method of claim 18, where the combinational test point comprises an OR gate.

27. The method of claim 18, where the combinational test point comprises an AND-OR gate.

28. An integrated circuit comprising at least one logic circuit and at least one delay fault circuit, the delay fault circuit including:

a first standard scan cell in a scan chain;

a combinational test point positioned immediately after the first standard scan cell in the scan chain; and

a second standard scan cell positioned immediately after the combinational test point in the scan chain.

29. The integrated circuit of claim 28, where the first and second scan cells are flip-flops.

30. The integrated circuit of claim 28, where the combinational test point is positioned to prevent shift dependency between the first standard scan cell and the second standard scan cell.

31. The integrated circuit of claim 28, where the combinational test point further comprises an AND gate, an OR gate, or an AND-OR gate.

32. A method for designing a circuit that is testable using a scan-based technique comprising:

accurately identifying, based on a functional analysis of the circuit, at least one pair of standard scan cells in the circuit where shift dependency occurs; and

inserting a test point at the identified point in the circuit.

33. The method of claim 32, where the inserted test points are dummy scan memories.

34. The method of claim 33, where the scan memories are flip-flops.

35. The method of claim 32, where the inserted test points are combinational gates.

36. The method of claim 32, where the points in the circuit where shift dependency occurs are identified using an automatic test program generator (ATPG).

37. The method of claim 36, where the ATPG identifies scan memories between which the test points are inserted.

38. The method of claim 37, where the scan memories are flip-flops.

39. A method of testing a circuit comprising:

a) applying a first set of two pattern tests using a skewed-load approach under standard scan environments;

b) applying a second set of two pattern tests that target faults that are not detected in step a using a broadside-load approach under standard scan environments; and

c) dividing test efforts required for remaining faults into a plurality of sub-phases and under each sub-phase enabling a different set of test points in every activation and propagation test cycle while the test points other than said different set of test points remain disabled.

40. The method of claim 39 where standard scan environments comprise testing environments where only a subset of all possible combination of test pattern pairs are applied to test the circuit.

41. The method of claim 39, where the circuit includes test points at points in the circuit where shift dependency occurs in a standard scan environment.

42. The method of claim 39, where during the skewed-load approach, a second pattern from the first set of two patterns is obtained by shifting in a first pattern from the two patterns by one scan memory element.

43. The method of claim 39, where during the broadside-load approach, a second pattern from the second set of two patterns is obtained by a response of the circuit to the first pattern.

44. The method of claim 39 where when test points are disabled for each first flip-flop and second flip-flop, the first and second flip-flops being adjacent in a scan chain, a value of the second flip-flop at a test cycle is maintained to be the same as a value of the second flip-flop at a previous test cycle.

45. The method of claim 39 where when a test point is enabled for each first flip-flop and second flip-flop, the first and second flip-flops being adjacent in a scan chain, a value of the second flip-flop at a test cycle is altered by the test point between the first and second flip-flops.

46. The method of claim 39, where at least two compatible test point signals are grouped together to be driven by a common control signal.

47. The method of claim 46, where at least a at least two inversely compatible test points are grouped together to be driven by a common control signal.

48. A method for designing test points for testing a circuit and identifying test points that should be enabled during each sub-phase of the testing, comprising:

a) identifying dependency untestable transition delay faults;

b) initializing global variables;

c) initializing a current test cube pair set and a current test point vector;

d) stopping the procedure if no more untested fault exists in a fault list;

e) selecting and marking an unmarked fault that has a minimum test generation cost in the fault list;

f) generating a test cube pair for the unmarked fault;

g) if the test cube pair generated in step f cannot be added to the current test cube pair set due to a conflict with any other test cube pair in the current test cube pair set, discarding the generated test cube pair and going to step e;

h) adding the generated test cube pair into the current test cube pair set and updating the current test point vector accordingly; and

i) if no more test cube pair can be added into the test cube pair set without conflict with other test cube pairs in the current test cube pair set, updating a global test point vector and going to step c.

49. The method of claim 48 where dependency untestable faults comprise faults that are not testable under standard scan environments but are testable under full enhanced scan environments.

50. The method of claim 49 where full enhanced scan environments comprise testing environments where all possible combination of test pattern pairs are applied to test the circuit.

51. The method of claim 49 where standard scan environments comprise testing environments where only a subset of all possible combination of test pattern pairs are applied to test the circuit.

52. The method of claim 48, where in step f a test cube pair is generated such that a minimum number of test points are generated considering the current test point vector and the global test point vector.

53. The method of claim 52, where the test cube pair is generated for two different time frames, one for an initialization pattern and another for a propagation pattern.

54. The method of claim 48, where when more than one backtrace is possible, a backtrace path that generates minimum controllability costs are used.

55. The method of claim 54, where controllability costs include a first time frame controllability cost and a second time frame controllability cost.

56. The method of claim 54, where controllability costs include hardware cost to be incurred when a line in the circuit is set to a binary value.

57. A method of claim 48, where a test pair is generated consider a test generation cost that is a sum of a controllability cost for an initialization, a controllability cost for activation and an observability cost which is a minimum cost for transferring an output of a propagated fault to a primary output of the circuit.